The workshop Report on Verilog HDL

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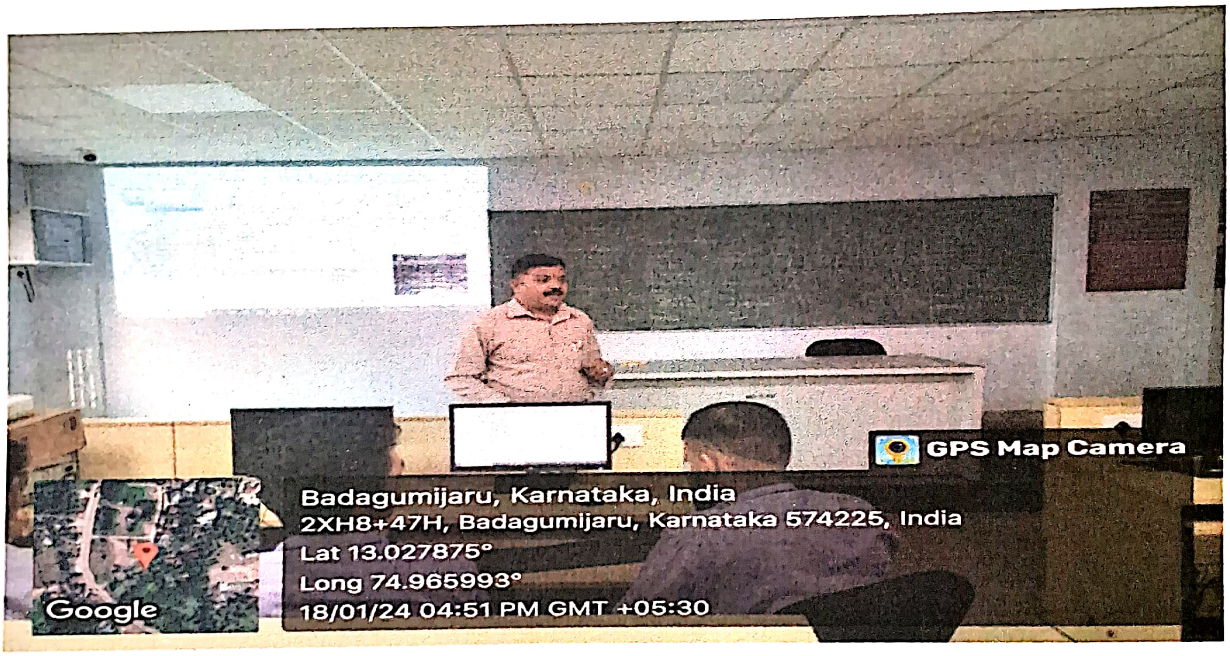
Introduction:

A Four-day workshop on Verilog HDL coding was organized by Dr. D V Manjunatha, Professor by Department of Electronics and Communication Engineering (ECE) and VLSI Club Coordinator at Alvas Institute of Engineering and Technology to the 3rd A/ Section Students scheduled on 17th to 18th of January, 2024 and 22nd to 23rd January, 2024. The program was aimed to provide participants with comprehensive knowledge and hands-on experience in Verilog coding in VLSI Design, covering both theoretical concepts and practical applications.



Objectives:

- To impart fundamental knowledge of Verilog Coding design principles.
- To introduce participants to various tools and methodologies used in Veilor Design.
- To provide hands-on experience through practical sessions.
- To enhance participants' understanding of current trends and advancements in Verilog design.

Agenda:

Day 1: Introduction to Verilog coding
Overview of Verilog Technology
Basic Building Blocks: Gates, Flip-Flops,
Introduction to HDL (Hardware Description Language)
Introduction to CAD Tools for Verilog Design Tools such Xilinx, VIAVADO ets.,
Day 2: Advanced VLSI Design
Combinational and Sequential Circuit Design

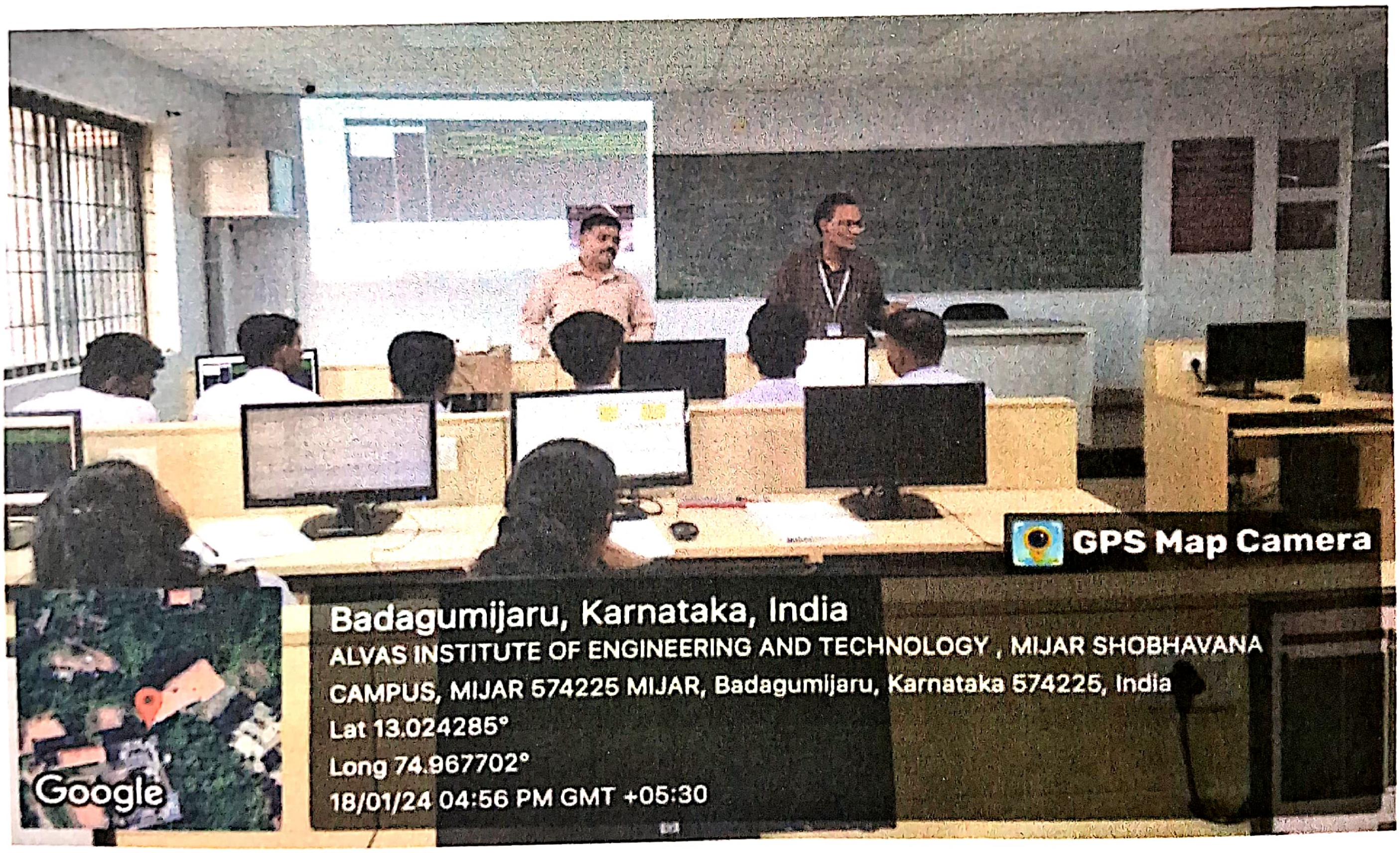
Introduction to FPGA (Field-Programmable Gate Array) Design
Hands-on Session: Designing Basic Circuits using CAD Tools
Day 3: Digital System Design with Xilinx EDA Tool, Register Transfer Level (RTL) Design Synthesis and Optimization Techniques, Timing Analysis.
Day 4: Emerging Trends and Future Directions, Introduction to System-on-Chip (SoC) Design, Low Power Design Techniques, Overview of VLSI Testing, Industry perspective: Challenges and Opportunities

Participants:

The work shop was conducted to all 3rd sem B/ Section Students to give the insight into the digital Design. The participants showed keen interest and active engagement throughout the sessions.

Outcome:

The workshop provided to be highly beneficial, achieving its objectives effectively. Participants gained a solid understanding of Verilog HDL coding principles, learned to use various CAD tools, and acquired practical skills through hands-on sessions. The interactive nature of the program encouraged active participation and knowledge sharing among participants.



Conclusion:

The Four-day workshop on Verilog HDL Dr. D V Manjunatha. Sr. Professor was a resounding success, providing participants with a comprehensive understanding of both HDL snd VLSI design concepts and practical skills. Such initiatives play a crucial role in bridging the gap between academia and industry, preparing participants for future challenges and opportunities in the field of VLSI technology.

Acknowledgments:

We extend our sincere gratitude to Dr. D V Manjunatha for his exemplary leadership and expertise in organizing this training program. Special thanks to all the participants for their enthusiastic participation and valuable contributions, which made the program a memorable learning experience for everyone involved.

D.V.

Dr. D.V. Manjunatha

VLSI Club Coordinator.

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